a channel region provided over said substrate between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a gate interconnect provided in a same layer as said gate electrode;

a metal layer comprising titanium provided over said substrate and being in direct contact with said gate interconnect and being connected with one of said source region and said drain region, said metal layer being connected with said gate interconnect through no contact hole;

an interlayer dielectric provided over said gate electrode and said metal layer;

a contact hole provided over said metal layer in said interlayer dielectric; and

a top layer interconnect comprising aluminum provided over said interlayer dielectric and connected with said metal layer through said contact hole.

74. (New) A semiconductor device comprising:

a substrate;

a source region and a drain region provided over said substrate;

a channel region provided over said substrate between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a gate interconnect provided in a same layer as said gate electrode;

a metal layer comprising titanium provided over said substrate and being in direct contact with said gate interconnect and being connected with one of said source region and said drain region;

an interlayer dielectric comprising silicon nitride provided over said gate electrode and said metal layer;

a contact hole provided over said metal layer in said interlayer dielectric; and

a top layer interconnect comprising aluminum provided over said interlayer dielectric and connected with said metal layer through said contact hole.

75. (New) A semiconductor device comprising:

a substrate;

a source region and a drain region provided over said substrate;

a channel region provided over said substrate between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a gate interconnect provided in a same layer as said gate electrode;

a metal layer comprising titanium provided over said substrate and being in direct contact with said gate interconnect and being connected with one of said source region and said drain region;

an interlayer dielectric comprising silicon oxide provided over said gate electrode and said metal layer;

a contact hole provided over said metal layer in said interlayer dielectric; and

a top layer interconnect comprising aluminum provided over said interlayer dielectric and connected with said metal layer through said contact hole.

76. (New) A semiconductor device comprising:

a substrate;

a source region and a drain region provided over said substrate;

a channel region provided over said substrate between said source region and said drain region;

a gate electrode comprising a doped polycrystalline silicon provided adjacent to said channel region with a gate insulating film therebetween;

a gate interconnect provided in a same layer as said gate electrode;

a metal layer comprising titanium provided over said substrate and being in direct contact with said gate interconnect and being connected with one of said source region and said drain region;

an interlayer dielectric provided over said gate electrode and said metal layer;

a contact hole provided over said metal layer in said interlayer dielectric; and

a top layer interconnect comprising aluminum provided over said interlayer dielectric and connected with said metal layer through said contact hole.

77. (New) The circuit of claim 60 wherein said thin film transistor is an n-channel thin film transistor.

78. (New) The circuit of claim 60 wherein said thin film transistor is a p-channel thin film transistor.

79. (New) The device of claim 73 wherein said contact hole is located outside said source region and said drain region.

80. (New) The device of claim 74 wherein said contact hole is located outside said source region and said drain region.

81. (New) The device of claim 74 wherein said metal layer is connected with said gate interconnect through no contact hole.

82. (New) The device of claim 75 wherein said contact hole is located outside said source region and said drain region.

83. (New) The device of claim 75 wherein said metal layer is connected with said gate interconnect through no contact hole.

84. (New) The device of claim 76 wherein said contact hole is located outside said source region and said drain region.

85. (New) The device of claim 76 wherein said metal layer is connected with said gate interconnect through no contact hole.--